CLAIMS:

1. A multiprocessor system, of the type comprising a central memory (RAM) organized in blocks of information (bi), treatment processors ($CPU_1 ... CPU_j ... CPU_n$), a cache memory ($MC_j$) connected to each treatment processor (CPU_j) and organized in blocks of information (bi) of the same size as those of the central memory, a directory (RG_j) and its management processor (PG_j) associated with each cache memory (MC_j), means for communicating addresses of blocks between processors (CPU_j) and the central memory (RAM), said multiprocessor system being characterized in that it is provided with:

an assembly of shift registers, called memory registers ($RDM_1 ... RDM_j ... RDM_n$), each register ($RDM_j$) of this assembly being connected to the central memory (RAM) in such a manner as to permit, in one cycle of this memory, a parallel transfer in read or write of a block of information (bi) between said register and said central memory,

shift registers, called processor registers ($RDP_1 ... RDP_j ... RDP_n$), each processor shift register (RDP_j) being connected to the cache memory (MC_j) of a processor (CPU_j) in such a manner as to permit a parallel transfer in read or write of a block of information (bi) between said shift register (RDP_j) and said cache memory (MC_j),

an assembly of series links ($LS_1 ... LS_j ... LS_n$), each connecting a memory shift register (RDM_j) and a processor shift register (RDP_j) and adapted to permit the transfer of blocks of information (bi) between the two registers considered (RDM_j, RDP_j).

2. A multiprocessor system as in Claim 1, characterized in that:

each memory shift register (RDM_j) and each processor shift register (RDP_j) are doubled into two registers, one specialized for transfer in one direction, the other for transfer in the other direction.

each series link (LS_j) comprising two unidirectional series links for transfer bib by bit, connecting the doubled memory shift r gister (RDM_j) and the corresponding doubled processor shift register (RDP_j), these links being connected to said registers for permitting, for one, a transfer in one direction, and for the other a transfer in the other direction:

3. A multiprocessor system as in Claim 1, characterized in that each series linek (LS_j) comprises a bidirectional link for bit by bit transfer, connected to the memory shift register (RDM_j) and to the corresponding processor shift register (RDP_j) and a validation logic (LV) for the direction of transfer in such a manner as to permit an alternate transfer in the two directions.

4. A multiprocessor system as in one of Claims 1, 2 or 3, characterized in that the address communication means comprises a common bus for parallel communication of addresses of blocks (BUSA) connecting the processors (CPU_j) and the central memory (RAM) and a bus arbitrator (AB) adapted to manage access conflicts on said bus.

5. A multiprocessor system as in Claim 4 one of Claims 1, 2 or 3, characterized in that the address communication means comprises a complementary shift register (RDC_j) connected on each ~~series~~ link (LS_j) in parallel with the corresponding memory shift register (RDM_j) in such a manner as to permit the transmission of addresses by the series links and their loading in said complementary shift registers (RDC_j), an access management ~~arbitrator~~ (ABM) being connected to said complementary shift registers (RDC_j) and to the central memory (RAM) in order to select the addresses contained in said registers (RDC_j) and to manage the access conflicts to the central memory (RAM).

6. A multiprocessor system as in one of Claims 1, 2, 3, 4 or 5, comprising means for managing the data shared between processors, in order to assure their coherence.

7. A multiprocessor system as in Claim 6, characterized in that the means for managing the shared data comprises>:

a special parallel communication bus for words (BUSD) connecting the processors (CPU_j) and the central memory (RAM),

a partition logic (LP_j), associated with each processor (CPU_j) and adapted to differentiate the addresses of shared data and those of non-shared data in such a manner as to transmit the same on the address communication means with their identification,

a decoding logic (DEC) associated with the central memory (RAM) and adapted to receive the addresses with their identification and direct the data in the memory output either to the corresponding memory shift register (RDM_j) for non-shared data, or to the special word communication bus (BUSD) for shared data.

8. A multiprocessor system as in Claim 6, characterized in that the shared data management means comprises, for one part, a special parallel word communication bus (BUSD) and a special common bus for communication of word addresses (BUSAM) connecting the processors (CPU_j) and the central memory (RAM), and for the other part a partition logic (LP_j) associated with each processor (CPU_j) and adapted to differentiate the addresses of shared data and those of non-shared data, in such a manner as to direct the former to the special common bus (BUSAM) and the latter to the means for communication of block addresses.

9. A multiprocessor system as in Claims 4 and 6 taken together, characterized in that the shared data management means comprises a memory management processor (PGM) associated with the central memory (RAM) and a snooper processor (PE_j) with a bus associated with each treatment processor (CPU_j) and the corresponding management directory (RG_j), each snooper processor (PE_j) with a bus and the memory management processor (PGM) being connected to the address communication bus (BUSA) in order respectively to supervise and treat the addresses of blocks transmitted on said bus in such a manner as to permit an updating of the central memory (RAM) and of the associated cache memory (MC_j) in case of detection of a block address present in the associated directory.

10. A multiprocessor system as in Claims 4 and 6 taken together, characterized in that the shared data management means comprises a memory management processor (PGM) associated with the central memory (RAM) and a coherence maintenance processor for shared data (PMC_j) associated with each treatment processor (CPU_j) and with the corresponding management directory (RG_j), each coherence maintenance processor (PMC_j) being connected to a synchronization bus (SYNCHRO) controlled by the memory management processor (PGM) in such a manner as to permit an updating of the central memory (RAM) and of the associated cache memory (MC_j) in case of detection of a block address, an updating of the central memory (RAM) and of the cache memories (MC_j) upon each selection of addresses on the common address bus BUSA.

11. A multiprocessor system as in Claims 5 and 6 taken together, characterized in that the shared data management means comprises a memory management processor (PGM) associated with the central memory (RAM) and a shared data coherence maintenance processor (PMC_j) associated with each treatment processor (CPU_j) and with the corresponding managing

directory (RG_j), each coherence maintenance processor (PMC_j) being connected to a synchronization bus (SYNCHRO) controlled by the memory management processor (PGM) in such a manner as to permit an updating of the central memory (RAM) and of the associated cache meory (MC_j) in case of detection of a block address, an updating of the central memory (RAM) and of the cache memories (MC_j) upon each address selection in the complementary shift registers (RDC_j).

12. A multiprocessor system as in one of Claims 1 to 11, characterized in that:

several processor shift registers (RDP_k, RDP_{k+1}...) corresponding to a given assembly of processors (CPU_k, CPU_{k+1}...) are connected in parallel to a same series link (LS_k), a local arbitrator being associated with each assembly of processors (CPU_k, CPU_{k+1}...) in order to arbitrate access conflicts to the series link (LS_k),

a memory management processor is connected to block address communication means and to the central memory (RAM) and comprises coding means adapted to associate with each block of information (BI) a leading identification of the processor concerned among each assembly (CPU_k, CPU_{k+1}...) sharing a series link (LS_k),

management processors (PG_k, PG_{k+1}...) associated with the cache memories (MC_k, MC_{k+1}...) of the processors of said assembly (CPU_k, CPU_{k+1}...) comprising decoding means for the leading identification.

13. A multiprocessor system as in one of Claims 1 to 12, characterized in that each memory shift register (RDM_j) is connected in a static manner to a series link (LS_j) specifically provided to said register.

14. A multiprocessor system as in one of Claims 1 to 12, characterized in that:

a memory management processosr (PGM) is associated with the central memory (RAM) and comprises a periodic block logic (ALLOC) for the memory shift registers to the series links,

the memory shift registers (RDM_1...RDM_j...RDM^n) are connected in a dynamic manner to the series links (LS_1 ...LS_j) by the intervention of an interconnection network (RI) controlled by the memory management processor (PGM).

15. A multiprocessor system as in one of Claims 1 to 14, in which the central memory (RAM) is constituted by m memory banks (RAM_1.. RAM_p...RAM_m) arranged in parallel, characterized in that each memory shift register comprises m elementary shift registers (RDM_{j1}...RDM_{jp}...RDM_{jm}) connected in parallel to the corresponding series link (LS_j), each elementary register (RDM_{jp}) being connected to a memory bank (RAM_p) in such a manner as to permit, in one cycle of said memory bank, a parallel transfer in reading or writing of a block of information (bi) between said elementary register and said memory bank.

16. A multiprocessor system as in Claim 15, in which each series link (LS_j) is divided into m series links (LS_{jp}), connecting point to point each processor (CPU_j) to the elementary shift register (RDM_{jp}).

17. A multiprocessor system as in Claim 15, in which each memory bank (RAM_p) is of the random access type provided with an input/output for data of a size corresponding to a block of information (bi), characterized in that said input/-output for each memory bank (RAM_p) is connected by a parallel bus to the assembly of elementary registers (RDM_{1p}... RDM_{jp}).

18. A multiprocessor system as in one of Claims 15, 16 or 17, synchronized by a clock of a frequency F at least equal to 100 megahertz, characterized in that each elementary memory shift register (RDM_{jp}) and each processor shift register (RDP_j) are of a type adapted to present a shift frequency at least equal to F.

19. A multiprocessor system as in one of Claims 15, 16 or 17, synchronized by a clock of a frequency F at least equal to 100 megahertz, characterized in that each elementary memory shift register and/or each processor shift register comprises an assembly of 2^u multiplexed sub-registers (RDM_{jp}, RDP_{jp}), each able to present a shift frequency at least equal to $F/2^u$.

20. A process for the exchange of information between a central memory (RAM) organized in blocks of information (bi) and processors (CPU_1,...CPU_j...CPU_n) each provided with a cache memory (MC_j) organized in blocks of the same size (bi), and a directory (RG_j) and its management processor (PG_j), in such a manner that the exchange between the central memory (RAM) and each processor (CPU_j) is carried out via the cache memory (MC_j) of the latter, said process being characterized in that each transfer of a block of information (bi) from the central memory (RAM) to the cache memory (MC_j) of a given processor consists of:

transferring in one cycle of the central memory, the block (bi) of said central memory (RAM) to a memory shift register (RDM_j) of the size of one block, making part of an assembly of shift registers (RDM_1...RDM_j...RDm_n) connected to the central memory,

transferring on a series link (LS_j) the contents of the memory shift register (RDM_j) to a processor shift register (RDP_j) of the same capacity, associated with the cache memory (MC_j) of the processor considered (CPU_j),

transferring the contents of said processor shift register (RDP_j) to said cache memory (MC_j).

21. A process for the exchange of information between a central memory (RAM) organized in blocks of information (bi) and processors ($CPU_1 \ldots CPU_j \ldots CPU_n$) each provided with a cache memory (MC_j) organized in blocks of the same size (bi), and a directory (RG_j) and its management processor (PG_j), in such a manner that the exchange between the central memory (RAM) and each processor (CPU_j) is carried out by the cache memory (MC_j) of the latter, said process being characterized in that each transfer of a block of information (bi) fromthe cache memory (MC_j) of a given processor (CPU_j) to the central memory consists of:

transferring the block (bi) of said cache memory considered (MC_j) to a processor shift register (RDP_j) of the size of one block, associated with said cache memory (MC_j),

transferring on a series link (LS_j) the contents of the processor shift register (RDP_j) to a memory shift register (RDM_j) of the same capacity, provided to the processor considered in an assembly of shift registers ($RDM_1 \ldots RDM_j \ldots RDM_n$) connected to the central memory (RAM),

transferring in one cycle of the central memory the contents of the memory shift register (RDM_j) to said central memory (RAM).

22. A multiport series memory component, capable of equipping a multiprocessor system according to one of Claims 1 to 19, characterized in that it comprises an integrated circuit comprising a random access memory (RAM) of a predetermined size corresponding to a block of information (bi), an assembly of shift registers ($RDM_1 \ldots RDM_j \ldots RDM_n$), each of a capacity corresponding to the size of the memory, an

internal parallel bus (BUSI) connecting the access of the memory and the shift registers, a shift register selection logic (LSR)adapted to validate the link on the internal bus between the memory and a predetermined shift register, and an assembly of external input/output pins (adbloc, admot, numreg, cs, wr, rd, bitbloc, normal/config, hi, di) for the input of addresses to the memory (RAM), for the input of addresses to the selection logic (LSR), for the input and the falidation of transfer commands in reading or writing of a block of information (bi) between the memory (RAM) and the shift registers (RDM_j), for the input of a clock signal to each shift register (RDM_j), for the bit by bit input of a block of information (bi) to each shift register (RDM_j) and for the bit by bit output of a block of information from each shift register (RDM_j).

23. A component as in Claim 22, characterized in that it comprises at least one configuration register (RC_1, RC_2...) having programming inputs, each configuration register being connected to a forcing logic (LF) connected to the memory (RAM) and to the shift registers (RDM_j) in order to assure the forcing of states of said memory and of said shift registers.

24. A component as in Claim 23, permitting the choice of the size of blocks of information (bi) treated, characterized in that:

the memory (RAM) is divided into zones combinable for permitting the sotrage of various possible sizes of blocks of information,

each shift register (RDM_j) is divided into combinable legs for permitting the loading of various possible sizes of blocks of information, with branches able to assure the corresponding shift for each size,

the internal bus (BUSI) is provided with a multiplexing logic (MT) for permitting the transfer of blocks of information (bi) of various sizes between the combinations of zones of the memory (RAM) and the corresponding combinations of legs of the shift registers (RDM_j),

a configuration register (RC_1) is provided with a capacity corresponding to the number of sizes of blocks possible,

the forcing logic (LF) connected to the register (RC_1) comprises a logic unit adapted to control the multiplexing logic (MT) in order to validate the transfers of blocks of information (bi) in a given size corresponding to the parameter contained on the configuration register (RC_1).

25. A component as on one of Claims 23 or 24, characterized in that:

the input and the output of each shift register (RDM_j) are connected to a same external pin by the intermediary of a logic gate (PL_j),

a configuration register (RC_2) is provided of a capacity corresponding to the number of shift registers (RDM_j),

the forcing logic (LF) connected to the configuration register (RC_2) comprises a logic unit adapted to control the logic gates (PL_j) in order to force the operation of each shift register (RDM_j) in the input mode or in the output mode as a function of a bit contained in the configuration register (RC_2) provided to said shift register (RDM_j).

26. A component as in one of Claims 23, 24 or 25, characterized in that:

the input and the output of each shift register (RDM_j) are connected to the same external pin by the intermediary of a logic gate (PL_j),

a configuration register (RC_3) is provided with a capacity corresponding to the number of shift regist rs (RDM_j),

the forcing logic (LF) connected to the configuration register (RC_3) comprises a logic unit connected to control the reading of the memory (RAM) and adapted to control each logic gate (PL_j) either in the output mode at the moment of reading of the memory (transfer of the memory RAM to the corresponding register RDM_j) during the entire duration of the emptying of said shift register (RDM_j), of in the input mode the remainder of the time.

27. A component as in one of Claims 23, 24, 25 or 26, characterized in that it comprises an external input pin (bit/bloc), one or more external data input/output pins, a control logic (COM) connected to the input pin (bit/bloc), to the data input/output pines, to the memory (RAM) and to the selection logic (LSR) and adapted according to the state of the input (bit/block) for generating either the transfers of blocks of information (bi) between memory (RAM) and shift registers (RDM_j), or the transfers of bits directly between the memory (RAM) and the data pins.

28. A component as in Claims 23 and 27 taken together characterized in that the configuration registers (RC_1, RC_2...) are connected:

to the selection logic (LSR) which is adapted for selecting said configuration registers for the predetermined addresses affected by said registers,

to the control logic (COM) which is adapted for transmitting the data originating from the data input/output pins to said configuration registers for their programming.

29. A component as in one of Claims 22 to 28, in which on the internal bus (BUSI) connecting the access of the memory (RAM) and the shift registers (RDM_j) is interposed a barrel shifter type logic (BS) adapted to assure a circular permutation on the bits of each block of information, said logic (BS) having a control input for the step of the shift in the word unit connected to the input pins (admot).